

## Claims

- [c1] 1. A re-oxidation process of a semiconductor device, comprising:  
 providing a substrate having a stacked structure thereon, wherein the stacked structure includes a polysilicon/tungsten silicide interface;  
 forming a CVD oxide layer on the substrate and the stacked structure with a chemical vapor deposition (CVD) process; and  
 performing an oxidation process to form a thermal oxide layer on the substrate and the stacked structure.
- [c2] 2. The re-oxidation process of claim 1, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a tunneling layer, a polysilicon floating gate, an inter-poly dielectric layer, a polysilicon control gate and a tungsten silicide layer.
- [c3] 3. The re-oxidation process of claim 1, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a gate dielectric layer, a polysilicon gate and a tungsten silicide layer.
- [c4] 4. The re-oxidation process of claim 1, wherein the CVD process is a low-pressure chemical vapor deposition (LPCVD) process or a plasma-enhanced chemical vapor deposition (PECVD) process.
- [c5] 5. The re-oxidation process of claim 1, wherein the CVD oxide layer is formed using silane ( $\text{SiH}_4$ ), tetraethyl-ortho-silane (TEOS) or dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) as a Si-source.
- [c6] 6. The re-oxidation process of claim 1, wherein the CVD oxide layer has a thickness from 30 Å to 120 Å.
- [c7] 7. The re-oxidation process of claim 1, wherein the oxidation process is conducted under  $\text{O}_2$ ,  $\text{H}_2\text{O}$  or  $\text{O}_2/\text{H}_2\text{O}$  atmosphere.
- [c8] 8. The re-oxidation process of claim 1, wherein the oxidation process is conducted in a batch-type or single wafer-type reaction chamber.
- [c9] 9. A method for fabricating a semiconductor device, comprising:

sequentially forming a tunneling layer, a first polysilicon layer, an inter-poly dielectric layer, a second polysilicon layer and a tungsten silicide layer on a substrate;

sequentially patterning the tungsten silicide layer, the second polysilicon layer, the inter-poly dielectric layer and the first polysilicon layer to form a stacked gate;

forming a CVD oxide layer on the substrate and the stacked gate with a chemical vapor deposition (CVD) process; and

performing an oxidation process to form a thermal oxide layer on the substrate and the stacked gate.

- [c10] 10. The method of claim 9, wherein the CVD process is a low-pressure chemical vapor deposition (LPCVD) process or a plasma-enhanced chemical vapor deposition (PECVD) process.
- [c11] 11. The method of claim 9, wherein the CVD oxide layer is formed using silane ( $\text{SiH}_4$ ), tetraethyl-ortho-silane (TEOS) or dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) as a Si-source.
- [c12] 12. The method of claim 9, wherein the CVD oxide layer has a thickness from 30 Å to 120 Å.
- [c13] 13. The method of claim 9, wherein the oxidation process is conducted under  $\text{O}_2$ ,  $\text{H}_2\text{O}$  or  $\text{O}_2/\text{H}_2\text{O}$  atmosphere.
- [c14] 14. The method of claim 9, wherein the oxidation process is conducted in a batch-type or single wafer-type reaction chamber.
- [c15] 15. A re-oxidation process of a semiconductor device, comprising:  
 providing a substrate having a stacked structure thereon, wherein the stacked structure includes a polysilicon/metal silicide interface;  
 forming a CVD oxide layer on the substrate and the stacked structure with a chemical vapor deposition (CVD) process; and  
 performing an oxidation process to form a thermal oxide layer on the substrate and the stacked structure.

- [c16] 16. The re-oxidation process of claim 15, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a tunneling layer, a polysilicon floating gate, an inter-poly dielectric layer, a polysilicon control gate and a metal silicide layer.
- [c17] 17. The re-oxidation process of claim 15, wherein the stacked structure includes a stacked gate that comprises, from bottom to top, a gate dielectric layer, a polysilicon gate and a metal silicide layer.
- [c18] 18. The re-oxidation process of claim 15, wherein the CVD process is a low pressure chemical vapor deposition (LPCVD) process or a plasma enhanced chemical vapor deposition (PECVD) process.
- [c19] 19. The re-oxidation process of claim 15, wherein the CVD oxide layer is formed using  $\text{SiH}_4$ , tetraethyl-ortho-silane (TEOS) or dichlorosilane ( $\text{SiH}_2\text{Cl}_2$ ) as a Si-source.
- [c20] 20. The re-oxidation process of claim 15, wherein the CVD oxide layer has a thickness from 30 Å to 120 Å.